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RESEARCH ARTICLE OPEN ACCESS

# 32nm Based High-Speed Low Calibrated Flash ADC comparator with improved ENOB

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***Abstract***
A 2-GS/s 6-bit streak simple to-computerized converter (ADC) in 90nm CMOS is displayed. Utilizing the reference-voltage- inserted adjustment lessens data transfer capacity prerequisites on the comparator to empower high examining rates with low power utilization. The ADC devours 28 mW and possesses 0.35 mm 2 . The proposed balanced strategy enhances ENOB from 3.0 to 5.1 with an info sinusoid at Nyquist recurrence.

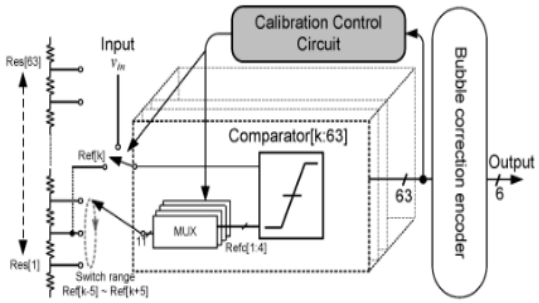
## I. Introduction

Numerous ADC architectures for low power application are made, in the same way as [1], [2]. For a few necessities, a high velocity, low power and midrange resolutions (e.g. 6 bits) are fundamental. It is a fundamental impediment to CMOS execution of ADC for wideband applications depends for the most part on attaining to a little include capacitance or huge transfer speed at the wanted precision. Attempting to decrease the data capacitance extra reactions for joined by enormous balance voltage, and the information capacitance specifically exchanges with the exactness. Also, since vital data adjustment exactness is not exactly a few mV without the preamplifier, so high-accuracy DACs are fundamental for all comparators. Be that as it may, high-exactness DACs circuits dependably expend a lot of force and this is not helpful for the configuration of low-power qualities. Including rapid, low power and high determination plan, we propose a 6-bit 2GS/s streak ADC in 90nm CMOS utilizing the reference-voltage-interjected alignment to diminish data transfer capacity necessities on the comparator to empower high inspecting rates with low power utilization.

## II. CIRCUIT D ESCRIPTION

### A. Architecture

As a rule, the nonlinearity of a blaze ADC normally comes about because of the irregular static and element counterbalance in the comparators. The balance in comparators gets to be more awful when the outlined size of information transistors is little for sparing force. Along these lines, numerous advanced adjustment strategies with great alignment extent and exactness are embraced. The majority of them build the parasitical capacitance in the air conditioner sign way in light of the fact that the impact of the additional parasitical capacitance will offer climb to additional force to hold the same information rate. As the necessity for information alignment exactness is not exactly a few mV without the preamplifier, high-accuracy DACs are essential for all comparators. Yet these DACs dependably expend a lot of force and this is not helpful for the configuration of low-power qualities. As per above reasons, we propose a straightforward and helpful system to make a comparator without an additional capacitive impact. Fig. 1 demonstrates the proposed ADC structural planning with an adjustment control circuit. Utilizing the reference resistor string initially displayed in the blaze ADC building design to give the aligned references does not deliver extra stacking impact while little transistor sizes and low power dissemination are considered.In view of the glimmer structural engineering, the proposed ADC can keep away from additional power as well as have precise alignment for high examining rate




Fig(1).proposed architecture of the 6b flash adc

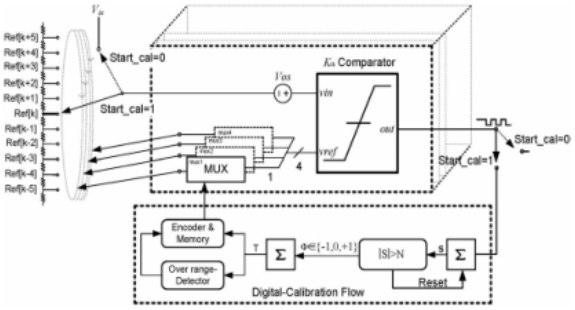



Fig. 2. Calibration flow for the comparator.

**B. Calibration Flow**

fig. 2 represents the alignment operation. On the off chance that the K th comparator is chosen into alignment stream, the begin sign of Start_cal turns into "1" to start doing the adjustment operation. The data gadget of the comparator associate with Ref[k] which is the first distributive reference voltage of K th comparator. The data gadget associated with the reference voltage is isolated into 4 sections (see Fig. 4). The yield balance extremity of the K th comparator is distinguished and gathered in S; the estimation of S is then sustained to a two-sided top locator (BTD). The BTD decides the estimation of Φ= {-1, 0, +1} as per whether S is more prominent than, littler than or between two level

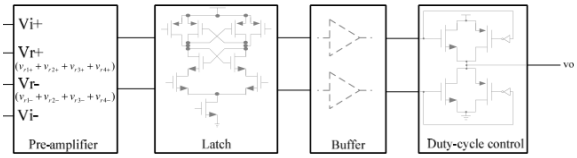



Fig. 3. Architecture of the comparator.

±N and afterward resets S. Next, the control signal T gathered structure Φ through encoder controls the multiplexers, mux1 to mux4. As per the extremity of comparator data counterbalance, each mux will move the reference voltage from Ref[k] to next one regulated. Assume that the information balance voltage of comparator, V os , is sure in the first place, mux1 to mux4 may move to Ref[k+1] regulated in positive course. In the first place, mux1 moves to interfaces with Ref[k+1] and the regardless others unite with Ref[k], and accordingly it gives 0.25 LSB to trim the +V os . Also, mux1 and mux2 interface with Ref[k+1] while mux3 mux4 still associate with Ref[k], bringing about 0.5 LSB to trim the +V os , et cetera. The location of balance extremity and counterbalance trimming continue working over and over to diminish +V os until +V os is near to 0 or the control word floods. The accompanying comparison can depict above case

$$Out = SGN\left[(V_{in} - V_r) \pm V_{os}\right] \approx SGN\left[(V_{in} - V'_r) \pm V_{os}\right] \pm V_{comp} \quad (1)$$

and

$$V'_r \pm V_{comp} = (V_{r1} + V_{r2} + V_{r3} + V_{r4})/4 \quad (2)$$

where V r1 , V r2 , V r3 and V r4 are the last associated reference voltages of mux1, mux2, mux3 and mux4, individually. Out can be spoken to as Out[T] with the file T showing trimming tally, and SGN is the sign capacity that relies on upon balance extremity and will give back 0 or 1. V 0 or § V comp V 0 r§ V comp is variable to take after the arbitrary V os.

**Simulation Analysis**

In Fig 3, the comparator comprises of the first stage completely differential preamplifier, the second stage differential hook, cradles and two ports to one port obligation cycle right circuit. The schematic of preamplifier is demonstrated in Fig. 4. where transistors M2 and M3 are partitioned into four equivalent sizes. The preamplifier has positive input transistors (M4, M5, M12 and M13) as a yield hook stage. This sort of lock is composed with low counterbalanced and force sparing than other sort of hooks. Kickback clamor and data basic mode voltage variety can be alleviated by the transistors M6 and M7. The fundamental voltage balance of the comparator is brought about by three variables: static counterbalance, element balance, and kickback commotion counterbalance. Static counterbalance results from procedure varieties (current component β and limit voltage V t ) and precise crisscrosses of gadgets. Element counterbalance is because of capacitive awkwardness of the lock

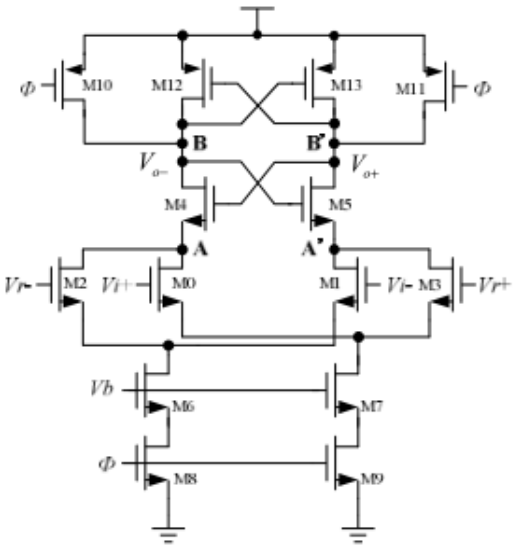



Fig. 4. Pre-amplifier of the comparator.

In the multi-stage comparator, the first phase of preamplifier decides the general counterbalance component. We will investigation for the first stage prelatch counterbalance. Taking due thought to the computerized alignment circuit many-sided quality and size of the territory, the choice of the revision extent has turned into a critical point. A few transistors can be discovered through the reference data [5] is especially expansive for the commitment to the information counterbalance voltage, and can be characterized as the affectability $S_{MX}^{V_{DS}}$. The info counterbalance voltage can be seen as the superposition of balance from every component. Utilizing the models of transistors gave by the fabricator, we acquire the accompanying data by Hspice reenactment that the information balance voltage significant donors by the transistors are M0 to M3 and M8 to M11 (Fig 4). In this work, the adjustment reach can cover no less than three standard deviations (3 σ ). As indicated by these varieties for the transistor and Monte-Carlo Reproduction results (Fig 5) for the comparator, the intuitive examination is given and afterward the transistor sizes are condensed in table I.To diminish the force utilization of the comparator, the sizes of the transistors are minimized to the detriment of vast counterbalance. In Fig 5, we run Monte-Carlo reenactments by the transistor models to gauge the most extreme counterbalance of the comparator. The model for this innovation has included the ability for confuse examination of the electrical parameters of an indistinguishable and nearly dispersed transistor pair. Attributes of the sigma of the confuse of V t and β , i.e. σδ V t and σδ β are demonstrated. In the meantime, some capacitance confound is likewise included into all Monte-Carlo reenactment to gauge the plausible jumble range. Furthermore, the capacitance contrasts Δ C AA' and Δ C BB' between the hubs An, An' and B, B' (Fig 4) are given 10% and 3σ standard deviation capacitance jumble, individually. As per thebalance voltage appropriation of a Gaussianbend in Fig. 5, its standard deviation σ is ascert ined as 1.3 LSB. It implies that 3σ is around 4 LSB and 99.7% balance voltage will be incorporated inside this extent. Considering the unpredictability and territory of advanced rationale circuits, we receive ±5 LSB as the adjustment range. The most extreme adjustment range ±5 LSB can contain the scope of 3.84σ stan

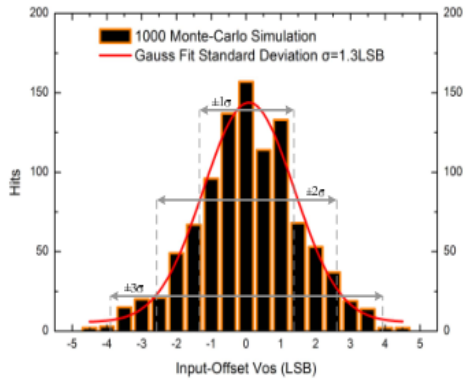



Fig. 5. Offset distribution of Monte-Carlo simulation.

Table I Transistor sizes of pre-amplifier

| Transistors | W/L |
|---|---|
| M0、M1、M2、M3 | 4/0.1 |
| M4、M5、M12、M13 | 2/0.1 |
| M8、M9、M10、M11 | 4/0.1 |

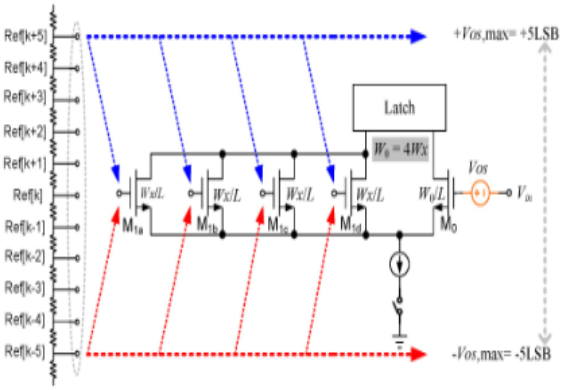
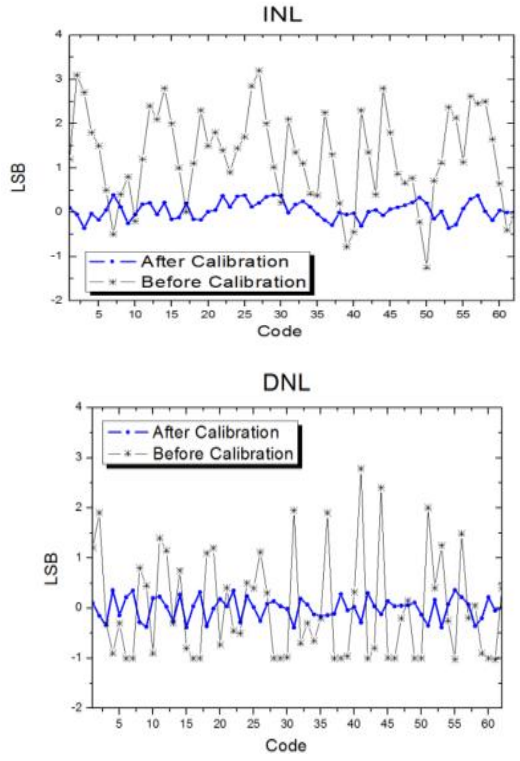



Fig. 6. Reference voltage calibration for the first stage of comparator.

**D. Reference Calibration for the Pre-amplifier**

Considering the greatest alignment extend, the data stage is acknowledged in Fig. 6. The source-coupled pair is utilized as the adjustment stage. The planned sizes for the balanced transistors are W 0/L = 4μm/0.1μm and W x/L = 1μm/0.1μm. Themtotal widths of M 1a , M 1b , M 1c and M 1d are equivalent to the width of M 0 . It uncovers that no any additional parasitic capacitance is included into comparator. Just additional multiplexers for reference voltages are included into ADC with less power utilization after adjustment. The aligned piece does not expand the parasitic capacitance on the sign way. The glimmer ADC itself utilizes the equivalent voltage parcels in the resistor string to give adjustment voltage levels, and subsequently no more needs an extra aligned voltage level from high-accuracy DACs circuits. After adjustment, the most piece of advanced alignment circuit determination off to spare force utilization but to keep the adjustment si




## III. CHIP IMPLEMENTATION AND MEASUREMENT RESULTS

To confirm the execution of the balanced blaze ADC as beforehand portrayed, the proposed circuit was manufactured in standard 90-nm CMOS innovation with an ostensible voltage of 1.2 V . It is conceivable to diminishing the utilization of switches and to bring down every entryway territory of switch in the outline of the comparator keeping in mind the end goal to unwinding the force utilization of clock cushions. To augment the ERBW, the design of info flag and clock sign to the comparators has been acknowledged by tree shape to minimize timing blunders. The alignment stream way is performed with DC info sign and underneath a low working pace (<50MS/s), and inspecting recurrence is still high recurrence at 2GS/s. Fig. 7 demonstrates the deliberate results for INL and DNL. Before adjustment, INL and DNL are about +3.3LSB to − 1.4LSB and +2.8LSB to − 1.2LSB, separately. After adjustment, INL and DNL are about +0.4LSB to − 0.39LSB and +0.36LSB to − 0.38LSB, separately. This alignment technique extraordinarily decreases INL and DNL, and advances linearity of this ADC. Fig. 8 exhibits that the SNDR is enormously enhanced from 22dB to 35dB and the change of ENOB is more prominent around 2 bits. The SNDR at low enter recurrence is around 35.6dB which compares to an ENOB of 5.6 bit. As the info recurrence is close Nyquist recurrence, its SNDR is enhanced from 19.6dB to 32.7dB. The ERBW which demonstrates SNDR drops by 3dB reaches out up to 0.76 GS/s. Chip micrograph is indicated in Fig. 9. Table II shows execution rundown and examination with earlier references [1], [3]

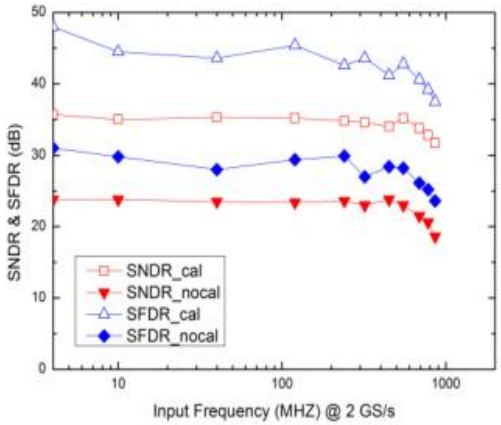



Fig. 8. SNDR versus $f_{in}$ at $f_{clk}$ = 2GS/s

## IV. CONSLUSION

Utilizing a standard 90-nm CMOS innovation, a 2-GS/s 6-bit streak ADC with reference-voltage inserted adjustment is exhibited. With the Monte-Carlo Recreation, we can gauge the attainable confuse range and focus balanced prerequisite. The ADC itself utilizes the voltage partitions in resistor string to give alignment levels without an extra aligned voltage level from high-accuracy DACs circuits. After adjustment, the most piece of computerized alignment circuit self discipline off to spare force utilization but to keep the adjustment signs. The proposed ADC can decrease transfer speed necessities on the comparator to empower high examining rates with low power utilization. The

ADC expends 28mW force and results in vitality every change Venture of 0.38 pJ/transformation step.
Affirmation: The creators might want to express gratitude toward NSC and CIC of Taiwan for money related and base

Table II Performance summary

| | Reference [1] | Reference [3] | Reference [4] | This Work | |
|---|---|---|---|---|---|
| Technology | 65 | 90 | 65 | 90 | nm CMOS |
| ENOB | 6 | 6 | 4.5 | 6 | Bit |
| Sampling frequency | 0.8 | 3.5 | 7.5 \| 6.25 | 2 | GS/s |
| Supply Voltage | 1.2 | 0.9 | 1.1 | 1.2 | V |
| Input range | NA | 1120 | 800 | 800 | mVp-p,diff |
| INL (after calibration) | < 0.5 | +0.96 ~ -0.39 | 0.38 | < ± 0.4 | LSB |
| DNL(after calibration) | < 0.5 | +0.5 ~ -0.48 | 0.35 | < ±0.38 | LSB |
| INL(before calibration) | > 2 | NA | 2.6 | +3.3 ~ -1.4 | LSB |
| DNL(before calibration) | > 2 | NA | 3.4 | +2.8 ~ -1.2 | LSB |
| ERBW | > 0.2 | NA | NA | 0.76 | GS/s |
| SNDR @ Nyquist-freq | > 33.1 | 31.18 | 25 \| 24.5 | 32.7 | dB |
| SNDR @ DC | 35.65 | 33.47 | 26 | 35.6 | dB |
| Power | 12 | 98 | 52 \| 47.5 | 28 | mW |
| Core Area | 0.13 | 0.15 | 0.065 x 0.162 | 0.35 | $mm^2$ |
| FOM | 0.4 | 0.95 | 0.497 \| 0.508 | 0.38 | pJ/conversion-step |

Note that $FOM = \frac{Power}{2^{ENOB}\left(2\ ERBW, f_{sample}\right)}$.

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